Claim(s)

We claim:

1. A method for verifying that a circuit described by a circuit specification as receiving and processing input signals to produce output signals has a property of responding to a first pattern in its input signals by producing a second pattern in its output signals within a finite time. the method comprising the steps of:

a. simulating operation of the circuit described by the circuit specification to produce output waveform data representing behavior of the circuit's input and output signals and representing a state of the circuit, wherein the output waveform data represents at least one occurrence of said first pattern in the input signals; and

b. determining a current state of the circuit from said output waveform data whenever the output waveform data represents an occurrence of the first pattern in the input signals, and

c. processing said circuit specification to determine whether, starting from each current state determined in step b, the circuit it describes will exhibit said second pattern within that finite time under all possible combinations of input signal states during said finite time.

2. An apparatus for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior occurring during clock cycles 1 - N of a clock signal following an antecedent event, wherein N is an integer greater than 0, wherein the circuit responds to input signals by producing output signals, wherein the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is production of a second state change pattern in at least one of the output signals, the apparatus comprising:

a circuit simulator for implementing a simulated circuit, wherein the simulated circuit simulates the circuit described by the circuit specification, wherein the circuit

simulator produces output waveform data representing time-varying behavior of the input and output signals and representing a current state of the simulated circuit;

detector means for detecting in the output waveform data an occurrence of a data pattern representing the antecedent event;

means for generating a temporally-expanded model of the simulated circuit representing the circuit as a set of N circuit functions CKT_1-CKT_N, each corresponding to a separate one of the N clock cycles.

3. The apparatus in accordance with claim 2 wherein the Kth circuit function CKT_K (for K = 1 to N) has a first input variable representing states of circuit input signals at a start of clock cycle K that influence the consequent behavior.

4. The apparatus in accordance with claim 3 wherein the Kth circuit function CKT_K (for K = 1 to N) has a second input variable representing states of circuit output signals at the start of clock cycle K that influence the consequent behavior.

5. The apparatus in accordance with claim 4 wherein the Kth circuit function CKT_K (for K = 1 to N-1) has a first output variable representing states of circuit output signals at an end of clock cycle K that influence the consequent behavior.

6. The apparatus in accordance with claim 5 wherein the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle k that are included in the second state change pattern.

7. The apparatus in accordance with claim 6 further comprising means for receiving and analyzing the second

output variable of each of the circuit functions to verify whether the circuit exhibits the consequent behavior.

8. A method for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior occurring during clock cycles 1-N of a clock signal following an antecedent event, wherein N is an integer greater than 0, wherein the circuit responds to input signals by producing output signals, wherein the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is production of a second state change pattern in at least one of the output signals, the method comprising the steps of:

a. simulating behavior of the circuit described by the circuit specification to produce output waveform data representing time-varying behavior of the input and output signals and representing a current state of the simulated circuit;

b. generating upon each occurrence of a data pattern in the output waveform data representing the antecedent event, a temporally-expanded model of the simulated circuit representing the circuit as a set of N circuit functions CKT_1-CKT_N, each corresponding to a separate one of the N clock cycles,

9. The apparatus in accordance with claim 8 wherein the Kth circuit function CKT_K (for K = 1 to N-1) has a first output variable representing states of circuit output signals at an end of clock cycle K that influence the consequent behavior.

10. The apparatus in accordance with claim 9 wherein the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle k that are included in the second state change pattern.

11. The apparatus in accordance with claim 10 further comprising means for receiving and analyzing the second output variable of each of the circuit functions to verify whether the circuit exhibits the consequent behavior.

12. The method in accordance with claim 11 wherein the Kth circuit function CKT_K (for K = 1 to N) has a first input variable representing states of circuit input signals at a start of clock cycle K that influence the consequent behavior.

13. The apparatus in accordance with claim 12 wherein the Kth circuit function CKT_K (for K = 1 to N) has a second input variable representing states of circuit output signals at the start of clock cycle K that influence the consequent behavior.

14. An apparatus for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior following an antecedent event, wherein the circuit responds to input signals by producing output signals, wherein the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is a second state change pattern in at least one of the output signals, the apparatus comprising:

a circuit simulator for implementing a simulated circuit, wherein the simulated circuit simulates the circuit described by the circuit specification, wherein the circuit simulator produces output waveform data representing time-varying behavior of the input and output signals and representing a current state of the simulated circuit;

detector means for detecting in the output waveform data an occurrence of a data pattern representing the antecedent event;

means for generating a state space model of the simulated circuit representing states of the simulated circuit that are reachable from the current state of the

simulated circuit represented by the circuit simulator output waveform data when the detector means detects the data pattern representing the antecedent event; and

means for analyzing the state space model to verify the circuit exhibits the consequent behavior.

15. The apparatus in accordance with claim 14

wherein the circuit transitions between states only on edges of a periodic clock signal supplied as input thereto,

wherein the consequent behavior occurs during a finite number of periods of the clock signal following the antecedent event, and

wherein the state space model represents all states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output data within the finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event.

16. The apparatus in accordance with claim 15 wherein the state space model represents all states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output data within the finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event.

17. A method for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior following an antecedent event, wherein the circuit responds to input signals by producing output signals, wherein the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is a second state change pattern in at least one of the output signals, the method comprising the steps of:

simulating the circuit to produce waveform data representing successive state changes of the input and output signals and representing successive states of the circuit;

generating a state space model of the circuit including states of the circuit that are reachable from a state of the circuit represented by the waveform data when the data represents the antecedent event; and

analyzing the state space model to verify the circuit exhibits the consequent behavior.

18. The method in accordance with claim 17

wherein the circuit transitions between states only on edges of a periodic clock signal supplied as input thereto,

wherein the consequent behavior occurs during a finite number of periods of the clock signal following the antecedent event, and

wherein the generated state space model includes all states of the circuit that are reachable from the current state of the circuit represented by the waveform data within the finite number of periods of the clock signal after the waveform data represents the antecedent event.

19. The method in accordance with claim 17 wherein the generated state space model includes only states of the circuit that are reachable from the current state of the circuit represented by the waveform data within the finite number of periods of the clock signal after the waveform data represents the antecedent event.